

Appl. No. 10/672,437
Amdt. Dated 03/28/2005
Reply to Office Action of October 29, 2004

REMARKS/ARGUMENTS

In response to the outstanding Office Action, one claim has been canceled and certain other claims have been amended.

In the Office Action, the Examiner objected to the drawings as not showing every feature of the invention specified in the claims. With respect to the objections related to claim 12, that claim has been carefully amended to eliminate the references to "switching converter" and the "controller circuit." With respect to the reference to "converter switching transistors," that reference has been changed to merely "switching transistors," which are already shown in the drawings. For instance, QH and QL in Figures 2, 3a and 4. Claims 14 and 27 have been amended to not specifically claim the synchronous rectifiers, but rather to claim the control output for coupling to control synchronous rectifiers. That control output is the PPWM output shown in Figure 3a and which is described starting on line 20 of page 18 of the application. In claim 15, references to the "converter output circuit" have been canceled.

Claims 8, 9, 12, 26 and 30 were rejected under 35 USC §112. Claim 8 has been amended to refer to the active source of power using the antecedent provided by claim 1. Claim 12 has also been amended to eliminate the reference to "switching converter" and the "controller circuit" and to provide an antecedent basis for simply "switching transistors," which as pointed out before, are transistors QH and QL in Figures 2, 3a and 4. Claim 26 has been amended to make clear that the transistor being referred to is the hot swap transistor specifically set out in claim 15. Claim 30 has been amended to not expressly claim the synchronous rectifiers, but rather to claim the generation of a control signal for coupling to control synchronous rectifiers, that control signal, as pointed out before, being the PPWM signal shown in Figure 3a.

In the Office Action, claims 1-4, 7-11, 15-18, 21-25, 28 and 29 were rejected under 35 USC §102(b) as being anticipated by Patel. Regarding claim 1, the Examiner equates the claimed hot swap transistor as transistor Q1 of Patel. This is not correct. "Transformer T1, transformer T2 along with transistors Q1, Q2, Q3, drive circuit 901 and control and drive circuit 902 form a square waveform 906 from the input voltage V_{in} as well as control the waveform's duty cycle." (column 12, starting on line 16) Thus, transistor Q1 is part of the pulse width modulator and clearly is not a hot swap transistor. Similarly, 901 is not part of any hot swap circuit, but rather is part of the pulse width modulator drive circuit. Further, the Examiner's statement that "the pulse width modulation switching regulator controller circuit and the hot swap circuit inherently being in a single integrated circuit" is clearly incorrect. "The I/O drawer is divided into two parts: a hot-plug region 730 and an embedded region 750." (column 6, starting on line 4) The drawers being referred to are drawers mounted within a standard 19 inch rack (see the Brief Description of the Drawings for Figure 6). Further, the hot swap region includes a plurality of ports and slots for connecting to other circuits. "Specifically, there are 2 ports 732-734 of the hot plug region dedicated to I/O port one (P1 of Fig. 5) and 6 slots 738-748 dedicated to I/O port two (P2 of Fig. 5)." (column 6, starting on line 24) Clearly, integrated circuits do not have ports and slots. In fact, in Figure 7 the hot-plug region 730 and the embedded region 750 are separated by a first I/O visor card 710. Accordingly, Patel clearly does not show a single integrated circuit.

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Regarding claims 2, 3 and 4, referring to Patel, the Examiner states that "the control voltage applied to the gate of transistor (Q1) increases to a predetermined rate to turn transistor (Q1) on." It has already been pointed out that Q1 is not a hot swap transistor. Further, as pointed out before, transistor Q1 is part of the circuitry that forms a square wave 906 from the input voltage V_{in} in controlling the waveform's duty cycle.

With respect to claim 7, it should be noted that because the error signal is maximum at startup, a pulse width modulator will normally start with a maximum pulse width and decrease until the output is within regulation. The undersigned could find nothing to the contrary in the portion of Patel referred to by the Examiner.

Regarding claims 8 and 9, the Examiner's comments with respect to element 1003 are not understood. Element 1003, in conjunction with resistor R2, determines the droop in the output voltage between no load and full load conditions. (See column 14, starting on line 18.) On claims 10 and 11, the undersigned can find no support for the Examiner's comments thereon.

With respect to claim 15, the comments made with respect to claim 1 also apply. Transistor Q1 is not a hot swap transistor, but rather is part of the square wave generator that generates the square wave 906. Further, the hot swap circuitry and the pulse width modulator circuitry are clearly independent circuits and not a single integrated circuit. These comments also apply to claims 16, 17 and 18 also.

With respect to claim 21, the undersigned finds no support for the Examiner's statement that in Patel "the PWM will start with a minimum pulse width and increase until the output of the PWM is within regulation" in the part of Patel referred to. When power is first applied to the circuit of Patel, the error amplifier signal will be at a maximum, as if a sudden and large load is applied. "Since the ramp signal is simply the output voltage, it is affected by any change in the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle as required." (column 12, starting on line 33) Since on first turn on the output voltage is way below regulation, the duty cycle should be the highest.

Regarding claims 22 and 23, claim 22 has been amended to make clear that the voltage referred to is not a PWM control voltage, but rather a voltage applied to the circuit as indicated by the voltage drop across the hot swap transistor falling below a predetermined voltage. Claim 23 adds the further limitation that the circuit will not start, even if the voltage across the hot swap transistor falls below a predetermined voltage, until the voltage exceeds a predetermined voltage. Claims 24 and 25 are similar to claims 22 and 23, though depend directly and indirectly from claim 15, rather than directly and indirectly from claim 22.

With respect claim 28, the same comments as made with respect to claim 1 apply. Transistor Q1 in Patel is not a hot swap transistor, but rather part of the square wave generator of the pulse width modulator. With respect to claim 29, the same comments apply as previously applied with respect to the rejection of claims 22 and 23.

With respect to the rejection of claims 15-18, 21, 22 and 28 under 35 USC §102(b) as being anticipated by Boylan, it is respectfully submitted that transistor 12 in Boylan is not a hot

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swap transistor, but rather a switching transistor as part of the pulse width modulator. Claim 15 specifically requires a hot swap transistor separate and apart from a pulse width modulation switching regulator controller. Claim 28 specifically requires that when voltage is first applied to the converter, increasing the voltage applied to the switching converter controller at a controlled rate. Boylan does not discuss the startup of the DC to DC converter disclosed therein, implying that when voltage is first applied to the converter, that full voltage is applied to the switching converter controller at the same time, not at a controlled rate. Accordingly, Boylan is not relevant to the present invention as claimed in these claims, the comments previously made with respect to these claims also being applicable here.

Claims 5, 6, 12, 13, 19, 20 and 26 were also rejected 35 USC §103(a) on Patel. It has already been pointed out numerous times herein that transistor Q1 of Patel is not a hot swap transistor, but rather, part of the pulse width modulator. Also, the Examiner states that "it would have been obvious to those skilled in the art to fabricate the circuit of Patel in integrated circuit form for cutting cost and reducing size." It is respectfully submitted, however, that this is simply hindsight reconstruction. Integrated circuits, pulse width modulation converter circuits and hot swap circuits are all well known in the prior art and have been commonly used for many years, yet the Examiner has not found any instances where a hot swap capability has been integrated with such a converter circuit. If it was truly obvious to do so, the Examiner should be able to cite numerous references showing the same. Without any such references, and the undersigned and inventor being unaware of any such references, this rejection is simply conclusional with no support in the prior art.

Information Disclosure Statements

Applicant filed an Electronic Information Disclosure Statement on January 23, 2004. Inasmuch as the outstanding Office Action does not contain an acknowledged copy of the Electronic Information Disclosure Statement, Applicant respectfully requests consideration of the same. A courtesy is attached hereto for the Examiner's convenience.

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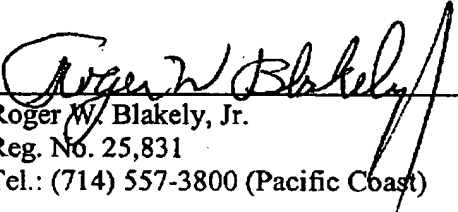
CONCLUSION

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 03/28/2005

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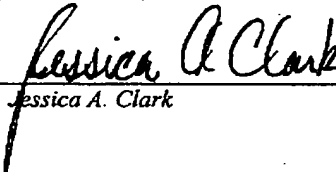
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